### SN54155, SN54156, SN54LS155A, SN54LS156, SN74155, SN74156, SN74LS155A, SN74LS156 DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS SDLS057 – MARCH 1974 – REVISED MARCH 1988

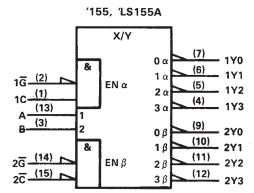
- Applications: Dual 2-to 4-Line Decoder Dual 1-to 4-Line Demultiplexer 3-to 8-Line Decoder 1-to 8-Line Demultiplexer
- Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words
- Input Clamping Diodes Simplify System Design
- Choice of Outputs: Totem Pole ('155, 'LS155A) Open-Collector ('156, 'LS156)

	TYPICAL AVERAGE	TYPICAL
TYPES	PROPAGATION DELAY	POWER
	3 GATE LEVELS	DISSIPATION
<b>'1</b> 55, <b>'156</b>	21 ns	125 mW
'LS155A	18 ns	31 mW
'LS156	32 ns	31 mW

#### description

These monolithic transistor-transistor-logic (TTL) circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. Input clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design.

#### logic symbols (2-line to 4-line decoder)<sup>†</sup>

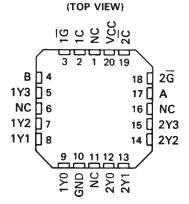


SN54155, SN54156, SN54LS155A, SN54LS156 . . . J OR W PACKAGE SN74155, SN74156 . . . N PACKAGE SN74LS155A, SN74LS156 . . . D OR N PACKAGE

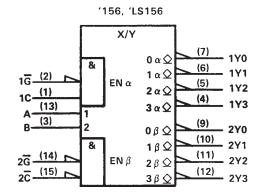
#### (TOP VIEW)

1C 1G B 1Y3 1Y2 1Y1 1Y0	<b>1</b> 2 3 <b>4</b> 5 <b>6</b>	U16 15 14 13 12 11		VCC 2C 2G A 2Y3 2Y2 2Y1
1Y0		10	6	2Y1
GND		9	6	2Y0

### SN54LS155A, SN54LS156 . . . FK PACKAGE



NC - No internal connection



<sup>†</sup>These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. For alternative symbols for other applications, see the following page.

Pin numbers shown are for D, J, N, and W packages.

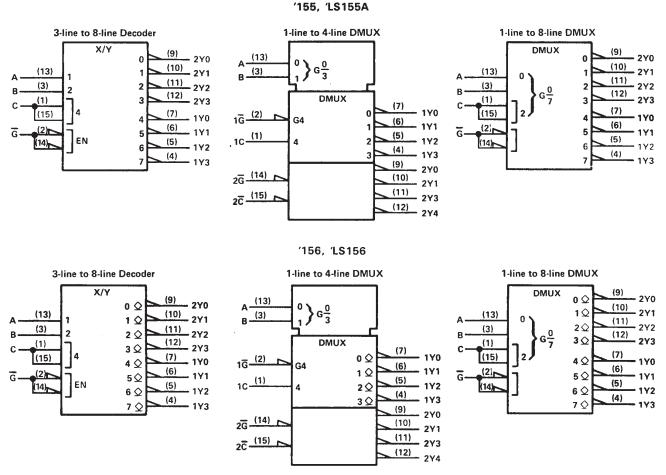
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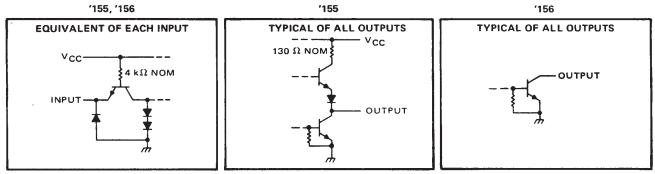
### SN54155, SN54156, SN54LS155A, SN54LS156, SN74155, SN74156, SN74LS155A, SN74LS156 **DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS** SDLS057 - MARCH 1974 - REVISED MARCH 1988

#### additional logic symbols (alternatives)<sup>†</sup>



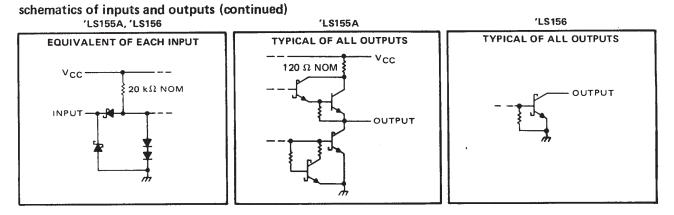
<sup>†</sup>These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

### schematics of inputs and outputs

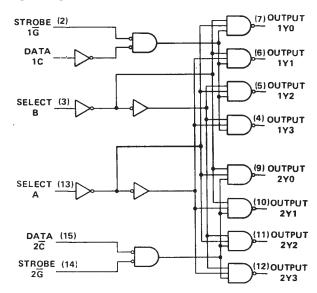




# SN54155, SN54156, SN54LS155A, SN54LS156, SN74155, SN74156, SN74LS155A, SN74LS156 **DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS** SDLS057 - MARCH 1974 - REVISED MARCH 1988



#### logic diagram (positive logic)



#### FUNCTION TABLES 2-LINE-TO-4-LINE DECODER **OR 1-LINE-TO-4-LINE DEMULTIPLEXER**

		INPUTS		OUTPUTS								
SEL B	ECT A	STROBE 1G	DATA 1C	1Y0	111	1¥2	1Y3					
X	х	н	X	н	н	н	н					
L	L	L	н	Ł	н	н	н					
L	н	L	(н	н	L	н	н					
н	L	L	н	н	н	L	н					
н	н	L	н	н	н	н	L					
х	x	x	Lι	н	н	н	н					

		INPUTS		OUTPUTS								
SEL B	ECT A	STROBE	DATA 2C	2Y0	2Y1	2Y2	2Y3					
х	х	н	×	н	н	н	Н					
L	L	L	L	L	н	н	н					
L	н	L	L	н	L	н	н					
н	ε	L	L	н	н	L	н					
н	н	L	L	н	н	н	L					
х	x	x	н	н	н	н	н					

#### FUNCTION TABLE 3-LINE-TO-8-LINE DECODER OR 1-LINE-TO-8-LINE DEMULTIPLEXER

		INP	UTS				OUTP	UTS			
SE	LEC	т	STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C‡	8	A	<u>G</u> ‡	2Y0	2Y1	272	2Y3	1Y0	1Y1	172	1¥3
х	х	х	н	н	н	н	н	н	н	н	н
L	L	L	L	L	н	н	н	н	н	н	н
L	£	н	L	н	Ł	н	н	н	н	н	н
L	н	L	L	н	н	L	н	н	н	н	н
L	н	н	L	н	н	н	Ł	н	н	н	н
н	L	L	L	н	н	н	н	Ł	н	н	Н
н	ι	н	ι	н	н	н	н	н	L	н	н
н	н	L	L	н	н	н	н	н	н	Ł	н
н	н	н	L	н	н	н	н	н	н	н	L

<sup>†</sup>C = inputs 1C and  $2\overline{C}$  connected together

 $\ddagger \overline{G} = inputs \ 1\overline{G} \ and \ 2\overline{G} \ connected \ together$ 

H = high level, L = low level, X = irrelevant



# SN54155, SN54156, SN54LS155A, SN54LS156, SN74155, SN74156, SN74LS155A, SN74LS156 DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)																															7 V
Input voltage: '155, '156																														•	5.5 V
'LS155A, 'LS156																															
Off-state output voltage: '156																		•									•				5.5 V
'LS156																															
Operating free-air temperature ran	ge:	SN	154	ľ, s	SN	54	LS	' C	irc	uit	s								•	•			•	•	•		-!	55	°C	to	125°C
		SN	174	¥', \$	SN	74	LS	' C	irc	uit	S	•	•	•	•			•	•	•		•	•	•	•	•	•	(	0°0	Ct	o 70°C
Storage temperature range		•		•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	• •	•	•	•	•	•			65	°C	to	150°C

NOTE 1: Voltage values are with respect to network ground terminal.

### recommended operating conditions

		SN5415	5		MIN NOM MAX 1.75 5 5.25			
	MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Supply voltage, V <sub>CC</sub>	4.5	5	5.5	4.75	5	5.25	V	
High-level output current, IOH			-800			-800	μA	
Low-level output current, IOL			16			16	mA	
Operating free-air temperature, T <sub>A</sub>	-55		125	0		70	°C	

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS <sup>†</sup>	1	SN54155 SN74155				
			MIN	TYP‡	MAX	]		
VIH	High-level input voltage		2			V		
VIL	Low-level input voltage				0.8	V		
VIK	Input clamp voltage	$V_{CC} = MIN, I_I = -8 mA$			-1.5	V		
Voн	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -800 µ	2.4	3.4		v		
VOL	Low-level output voltage	V <sub>IL</sub> = 0.8 V, I <sub>D</sub> H = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>D</sub> L = 16 mA	<u>-  </u>	0.2	0.4	v		
η · · ·	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>1</sub> = 5.5 V			1	mA		
Чн	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V			40	μA		
1 <sub>L</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-1.6	mA		
laa	Short-circuit output current§	SN54155	-20		-55			
los		V <sub>CC</sub> = MAX SN74155	-18		-57	mA		
	Supply autont	V <sub>CC</sub> = MAX, SN54155		25	35			
1CC	Supply current	See Note 2 SN74155		25	40	mA		

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ} \text{ C}$ .

\$ Not more than one output should be shorted at a time.

NOTE 2: I<sub>CC</sub> is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

# switching characteristics, $V_{CC} = 5 V$ , $T_A = 25 °C$

PARAMETER	FROM	то	LEVELS	TEST CONDITIONS		N5415		UNIT
	(INPUT)	(OUTPUT)	OF LOGIC		MIN	TYP	MAX	
<sup>t</sup> PLH	A, B, 2C, 1G, or 2G	Y	2			13	20	ns
tPHL,	A, B, 2C, 1G, or 2G	Y	2	C <sub>L</sub> = 15 pF,		18	27	ns
tPLH	A or B	У	3	$R_L = 400 \Omega$ , See Note 3		21	32	ns
<sup>t</sup> PHL	A or B	Y	3	See Note 3		21	32	ns
tPLH	10	Y	3			16	24	ns
tPHL	1C	Y	3			20	30	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



# SN54155A, SN74155A **DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS**

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#### recommended operating conditions

		SN5415	6	5			
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V <sub>CC</sub>	4.5	5	5.5	4.75 <sup>•</sup>	5	5.25	V
High-level output voltage, VOH			5.5			5.5	V
Low-level output current, IOL			16			16	mA
Operating free-air temperature, TA	-55		125	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS <sup>†</sup>		SN54156 SN74156					
			MIN	TYP‡	МАХ				
VIH	High-level input voltage		2			V			
VIL	Low-level input voltage				0.8	V			
VIK	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>1</sub> =8 mA			-1.5	V			
юн	High-level output current	$V_{CC} = MIN, V_{IH} = 2 V,$			250	μΑ			
чОн	rightever output current	V <sub>IL</sub> = 0.8 V, V <sub>OH</sub> = 5.5 V			200				
VOL	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,		0.2	0.4	v			
VOL	Low-level output voltage	VIL = 0.8 V, IOL = 16 mA		0.2	0.1	·			
Ц	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1	mA			
ПН	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V			40	μA			
11L	Low-level input current	V <sub>CC</sub> = MAX, V <sub>1</sub> = 0.4 V			1.6	mA			
		V <sub>CC</sub> = MAX, SN54156		25	35				
1CC	Supply current	See Note 2 SN74156		25	40	- mA			

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. <sup>‡</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C. NOTE 2: I<sub>CC</sub> is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

#### SN54156 то **LEVELS** FROM PARAMETER§ **TEST CONDITIONS** SN74156 **OF LOGIC** (INPUT) (OUTPUT) MAX MIN TYP A, B, 2<del>C</del>, 23 Y 2 15 <sup>t</sup>PLH 1G, or 2G A, B, 2C, 20 30 Y 2 $C_L = 15 \text{ pF},$ <sup>t</sup>PHL $1\overline{G}$ , or $2\overline{G}$ $R_L = 400 \Omega$ , 23 34 A or B 3 <sup>t</sup>PLH Y See Note 3 23 34 3 A or B Y <sup>t</sup>PHL 27 18 1C Y 3 **tPLH** 33 22 1C Y 3 <sup>t</sup>PHL

### switching characteristics, VCC = 5 V, TA = 25 °C

§tPLH = propagation delay time, low-to-high-level output

tpHL = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



UNIT

ns

ns

ns

ns

ns

ns

# SN54LS155A, SN74LS155A DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

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### recommended operating conditions

	SN	54LS1	55A	SN	74LS15	55A	
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V <sub>CC</sub>	4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH			400			-400	μA
Low-level output current, IOL			4			8	mA
Operating free-air temperature, TA	-55		125	0		70	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			SN	SN54LS155A		SN74LS155A		55A	UNIT	
PARAMETER	TES	TEST CONDITIONS <sup>†</sup>		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
VIH High-level input voltage				2			2			V
VII Low-level input voltage						0.7			0.8	V
VIK Input clamp voltage	V <sub>CC</sub> = MIN,	I <sub>I</sub> = -18 mA				-1.5			-1.5	V
VOH High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = V <sub>IL</sub> max	V <sub>IH</sub> = 2 V, , I <sub>OH</sub> = -400 μ/	4	2.5	3.4		2.7	3.4		v
		V <sub>IH</sub> = 2 V,	IOL = 4 mA		0.25	0.4		0.25	0.4	l v
VOL Low-level output voltage	VIL = VIL max	c	IOL = 8 mA					0.35	0.5	
Input current at Input current at maximum input voltage	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 7 V				0.1			0.1	mA
IIH High-level input current	V <sub>CC</sub> = MAX,	VI = 2.7 V				20			20	μΑ
IL Low-level input current	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 0.4 V				-0.4			-0.4	mA
IOS Short-circuit output current§	V <sub>CC</sub> = MAX			- 20		- 100	- 20		- 100	) mA
ICC Supply current	V <sub>CC</sub> = MAX,	See Note 2			6.1	10		6.1	10	) mA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

 $\$  Not more than one output should be shorted at a time.

NOTE 2: I<sub>CC</sub> is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

PARAMETER	FROM	то	TEST CONDITION			SN54LS155A SN74LS155A		
	(INPUT)	(OUTPUT) OF LOG	OF LOGIC		MIN	түр	МАХ	
<sup>t</sup> РLН	A, B, 2Ē, 1Ē, or 2Ē	Y	2			10	15	ns
<sup>t</sup> PHL	A, B, 2Ē, 1Ē, or 2Ē	Y	2	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ,		19	30	ns
tPLH	A or B	Y	3	See Note 3		17	26	ns
tPHL	A or B	Y	3	oce note o		19	30	ns
tPLH	1C	Y	3			18	27	<u> </u>
<sup>t</sup> PHL	1C	Y	3			18	27	ns

### switching characteristics, $V_{CC} = 5 V$ , $T_A = 25^{\circ}C$

 $f_{tPLH}$  = propagation delay time, low-to-high-level output

tpHL = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



# SN54LS156A, SN74LS156A DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

#### recommended operating conditions

	SI	SN541,S156			SN74LS156		
	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC</sub>	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, VOH			5.5			5.5	V
Low-level output current, IOL			4			8	mA
Operating free-air temperature, TA	55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		_			SI	V54LS1	56	SN74LS156			UNIT
PARAMETER		TEST	TEST CONDITIONS <sup>†</sup>		MIN TYP <sup>‡</sup> 1		MAX	MIN	түр‡	MAX	
VIH	High-level input voltage				2			2			V
VIL	Low-level input voltage						0.7			0.8	V
VIK	Input clamp voltage	V <sub>CC</sub> = MIN,	l <sub>l</sub> = –18 mA				-1.5			-1.5	V
юн	High-level output current	V <sub>CC</sub> = MIN, V <sub>IL</sub> = V <sub>IL</sub> max,	V <sub>IH</sub> = 2 V, V <sub>OH</sub> = 5.5 V				100			100	μA
VOL	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = V <sub>IL</sub> max	V <sub>IH</sub> = 2 V,	I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 8 mA		0.25	0.4		0.25 0.35	0.4	4 V
ų	Input current at maximum input voltage	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 7 V				0.1			0.1	mA
ЧН	High-level input current	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 2.7 V				20			20	μA
<u>цг</u>	Low-level input current	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 0.4 V				-0.4			-0.4	mA
Icc	Supply current	V <sub>CC</sub> = MAX,	See Note 2			6.1	10		6.1	10	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. <sup>†</sup> the value location of  $M_{10} = 5 M_{10} = 25^{\circ} C$ 

<sup>‡</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C. NOTE 2: I<sub>CC</sub> is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

PARAMETER§	FROM TO	1		TEST CONDITIONS	SN54LS156 SN74LS156			UNIT
	(INPUT)	PUT) (OUTPUT) OF LOGIC		MIN	ТҮР	MAX		
<sup>t</sup> PLH	A, B, 2Ē 1Ē, or 2Ē	Y	2			25	40	ns
<sup>t</sup> PHL	A, B, 2Ē, 1 <u>G</u> , or 2 <u>Ē</u>	Y	2	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ,		34	51	ns
tPLH	A or B	Y	3	See Note 3		31	46	ns
tPHL	A or B	Y	3	See Note 3		34	51	ns
tPLH	1C	Y	3			32	48	ns
tPHL	1C	Y	3			32	48	ns

### switching characteristics, $V_{CC} = 5 V$ , $T_A = 25^{\circ}C$

 ${}^{\$}$ tPLH = propagation delay time, low-to-high-level output

tpHL = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

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Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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		Wireless	www.ti.com/wireless

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Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

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Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

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Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
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		Wireless	www.ti.com/wireless



TEXAS INSTRUMENTS www.ti.com

18-Sep-2008

### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9750801Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9750801QEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9750801QEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9750801QFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
5962-9750801QFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SN54155J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN54155J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN54LS155AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS155AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS156J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS156J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN74155N	OBSOLETE	PDIP	Ν	16		TBD	Call TI	Call TI
SN74155N	OBSOLETE	PDIP	Ν	16		TBD	Call TI	Call TI
SN74155N3	OBSOLETE	PDIP	Ν	16		TBD	Call TI	Call TI
SN74155N3	OBSOLETE	PDIP	Ν	16		TBD	Call TI	Call TI
SN74156N	OBSOLETE	PDIP	Ν	16		TBD	Call TI	Call TI
SN74156N	OBSOLETE	PDIP	Ν	16		TBD	Call TI	Call TI
SN74LS155AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155AN	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS155AN	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
						. /		

# PACKAGE OPTION ADDENDUM

CU NIPDAU

Lead/Ball Finish MSL Peak Temp (3)

CU NIPDAU N / A for Pkg Type

Level-1-260C-UNLIM

18-Sep-2008

WWW.ti.com						PACKAG	E
Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Packag Qty	e Eco Plan <sup>(2)</sup>	L
						(RoHS)	
SN74LS155ANE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	
SN74LS155ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	ĸ
SN74LS155ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	k
SN74LS155ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	ĸ
SN74LS155ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	k
SN74LS155ANSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	k
SN74LS155ANSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	k
SN74LS156D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	k
SN74LS156D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	ĸ
SN74LS156DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	k
SN74LS156DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	k
SN74LS156DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	ĸ
SN74LS156DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	k
SN74LS156DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	ĸ
SN74LS156DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	k
SN74LS156DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS &	ĸ

SN74LS156DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156N	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS156N	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS156N3	OBSOLETE	PDIP	Ν	16		TBD	Call TI	Call TI
SN74LS156N3	OBSOLETE	PDIP	Ν	16		TBD	Call TI	Call TI
SN74LS156NE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS156NE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS156NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

18-Sep-2008

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Packag Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LS156NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54155J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ54155J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ54155W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI
SNJ54155W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI
SNJ54LS155AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS155AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS155AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS155AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS155AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS155AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS156FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54LS156FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54LS156J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS156J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS156W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS156W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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# PACKAGE OPTION ADDENDUM



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### TAPE AND REEL INFORMATION





# QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal Device	Package	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS155ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS155ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS156DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS156NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1



# PACKAGE MATERIALS INFORMATION

19-Mar-2008



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS155ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS155ANSR	SO	NS	16	2000	346.0	346.0	33.0
SN74LS156DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS156NSR	SO	NS	16	2000	346.0	346.0	33.0

MLCC006B - OCTOBER 1996

### FK (S-CQCC-N\*\*)

### LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



## MECHANICAL DATA

### PLASTIC SMALL-OUTLINE PACKAGE

### 0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 $\bigcirc$ Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS \*\* 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G\*\*)

**14-PINS SHOWN** 

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



J (R-GDIP-T\*\*) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.



D(R-PDSO-G16)



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



# N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- $\triangle$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



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